

Automated And Predictable Design Closure With In-Design Physical Verification



*Plug in to **SAMSUNG**
Preview the Possibilities*

**Harpreet Gill
Santhosh Pillai**

**System LSI SoC R&D
Samsung Electronics**

**June 14th 2010
Design Automation Conference**

SAMSUNG

ELECTRONICS

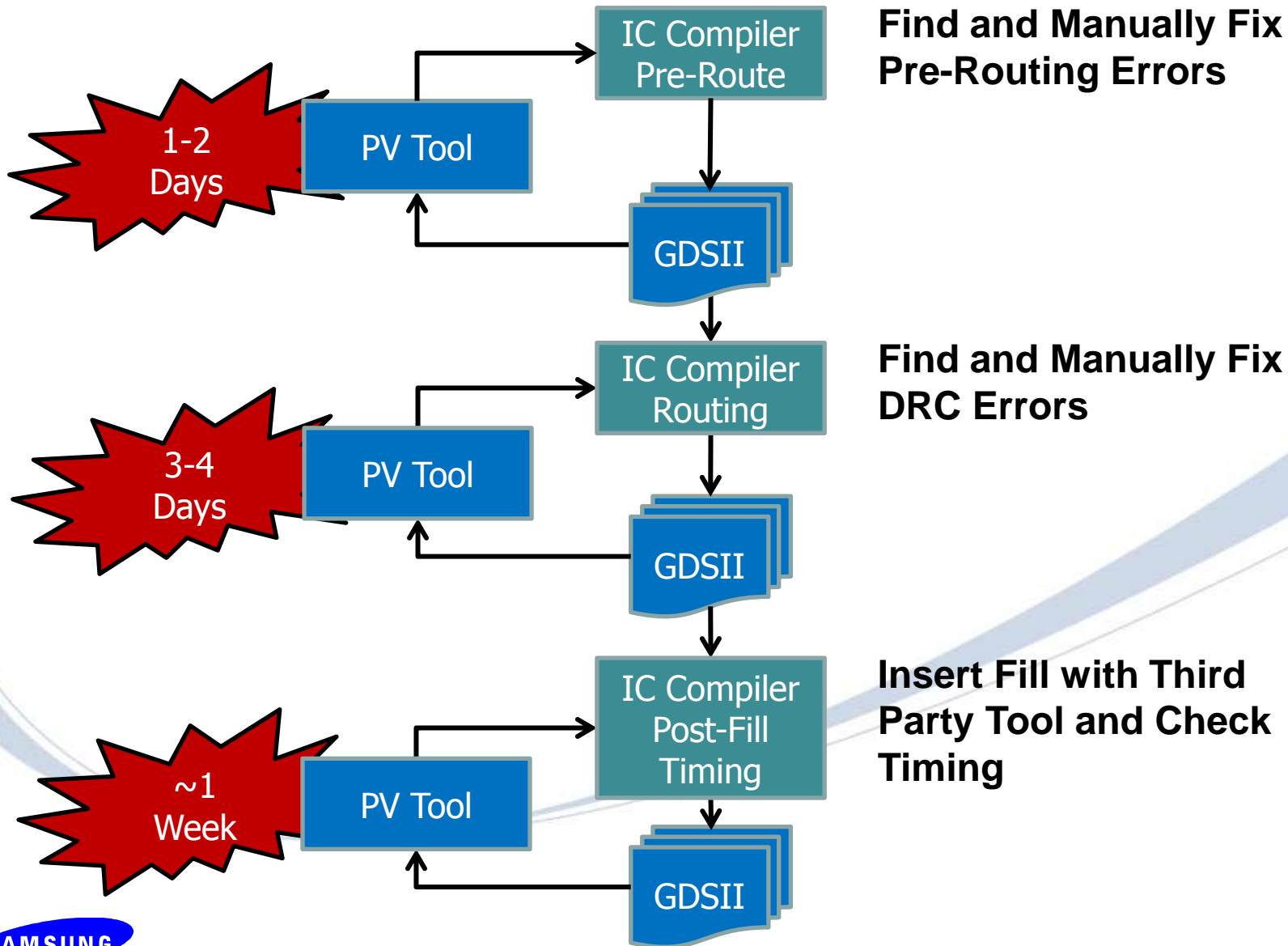
Agenda

Team Charter

- **Current Implementation Flow**
- **Synopsys In-Design Physical Verification Flow**
 - Pre-Route Power-Ground Checks
 - Automatic DRC Repair
 - Metal Fill
- **Summary and Next Steps**

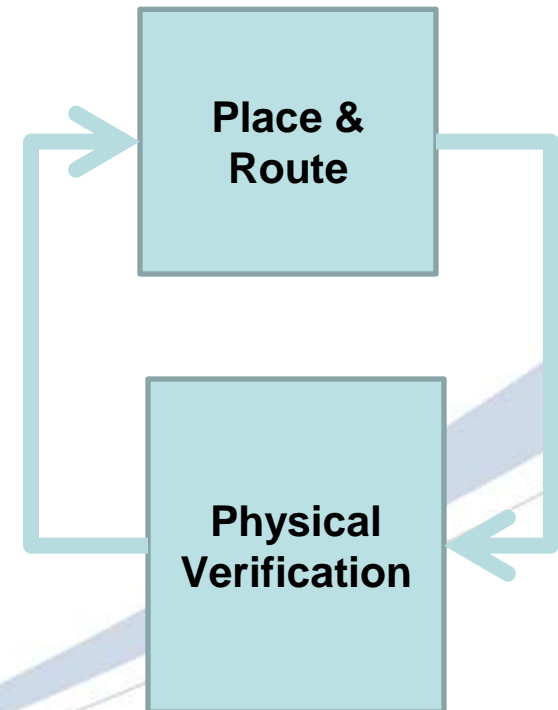
- **Physical Design of Complex SoCs**
 - 15 designers and growing
 - 2-3 designs per year
 - Hierarchical designs with several blocks
 - Block-level and top-level closure
- **Responsible for P&R, Extraction, Timing, Electrical Signoff and Physical Verification**
- **Seeking Automated and Predictable Ways to Get Faster Backend Design closure**

Current Implementation Flow



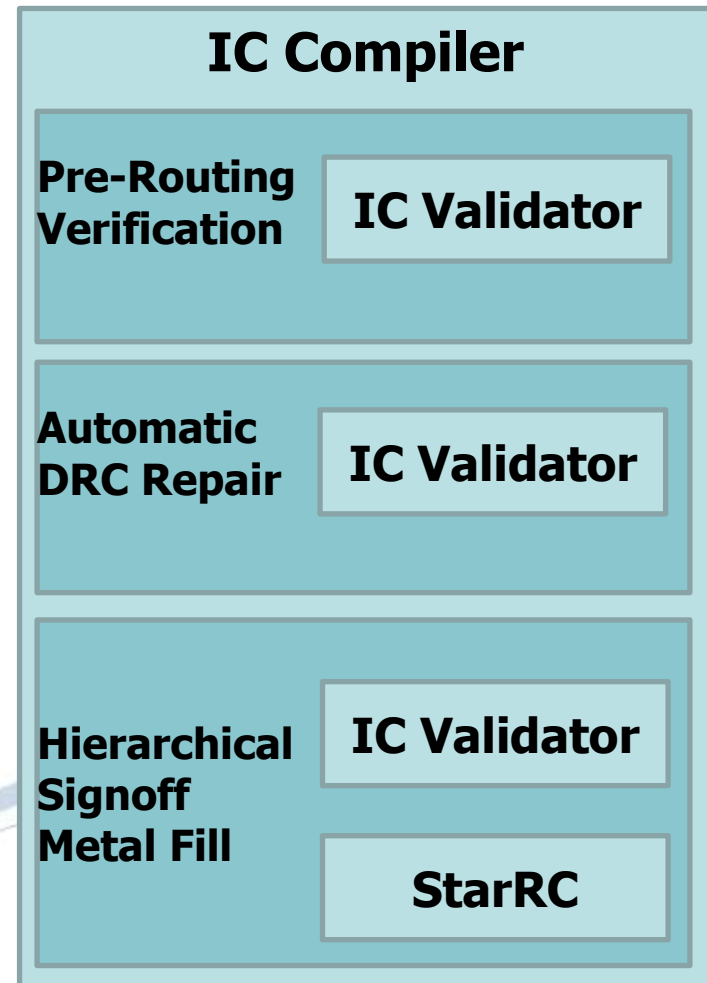
Opportunities to Enhance the Current Flow

- **Flag Pre-Routing Errors Early to Prevent Rip up and Re-route Later in the Flow**
- **Assistance in Fixing Outlier DRC Errors**
- **Insert Hierarchical, Signoff Fill During Design**
 - Eliminates timing issues
 - Faster runtime
 - No stream out
 - In production at Samsung



In-Design Physical Verification Flow with IC Validator

- **Signoff Runset Driven**
- **IC Compiler Centric**
 - No need to learn physical verification tool
- **Automated DRC Correction**
- **Hierarchical Metal Fill**
- **Fast Runtime**



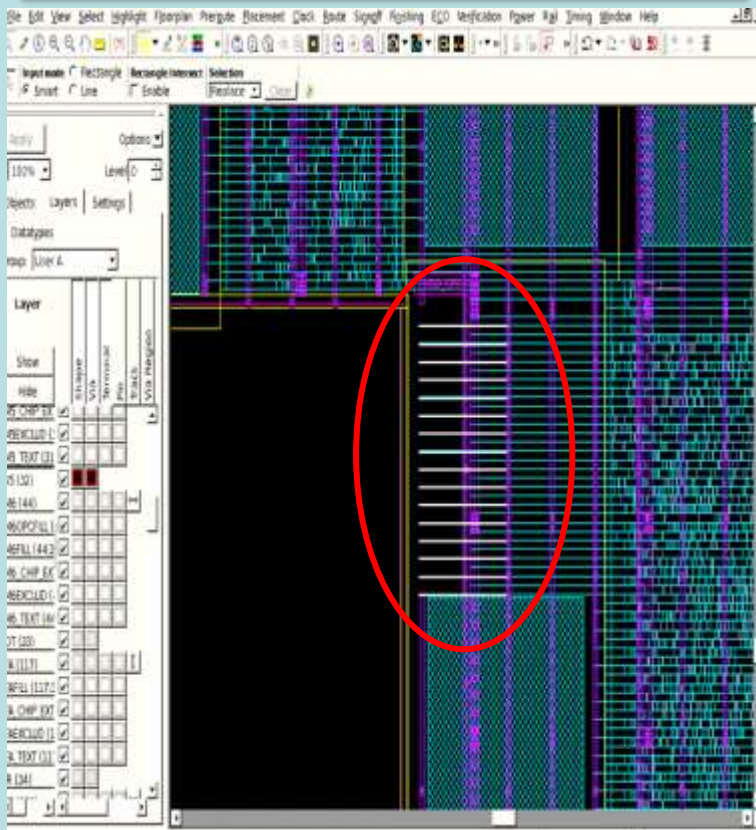
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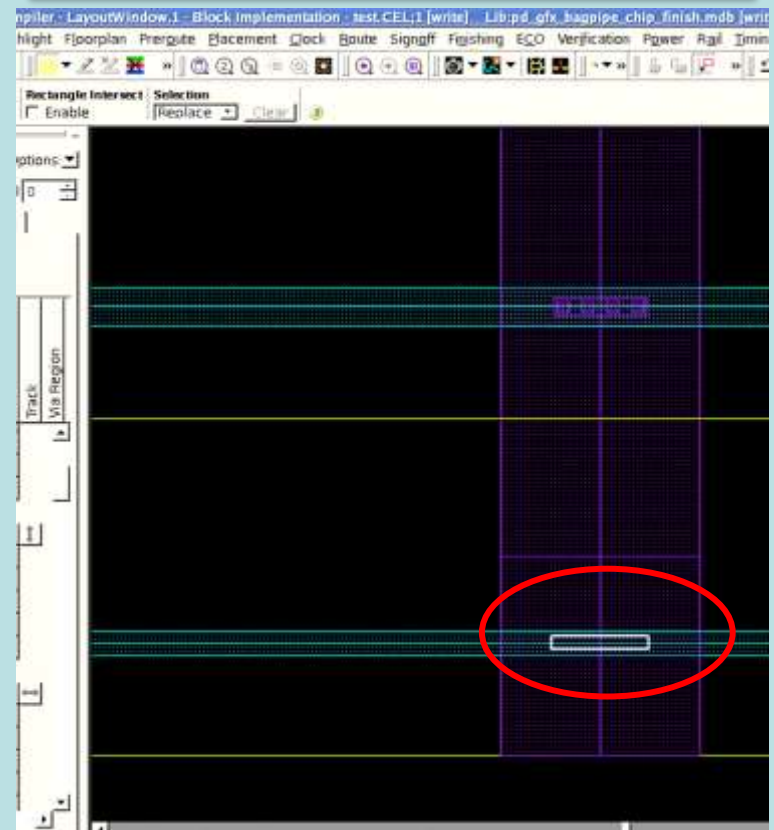
Pre-Routing Verification

Early Detection Eliminates Last-Minute Surprises

Dangling Power Ground Nets



Missing VIA Enclosures



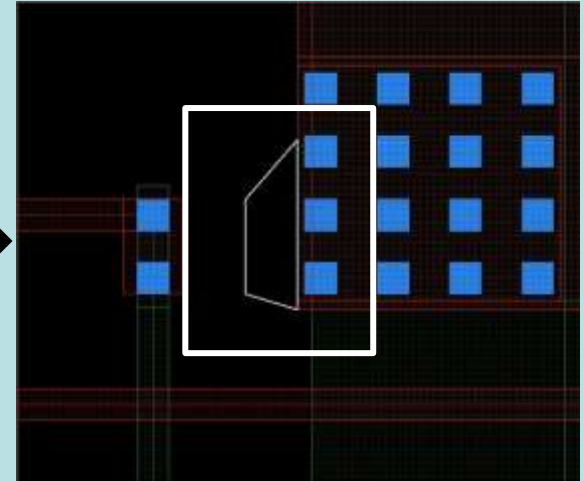
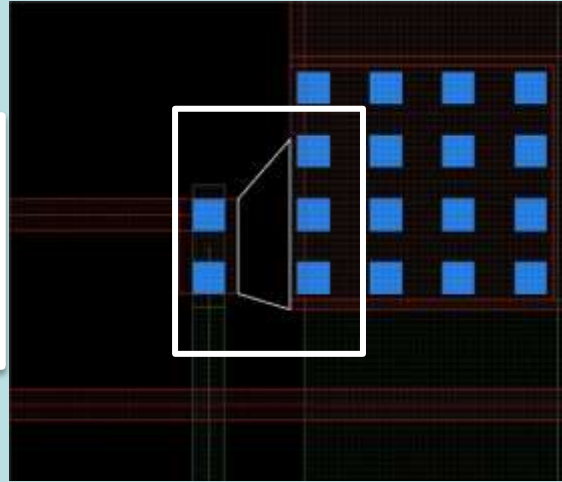
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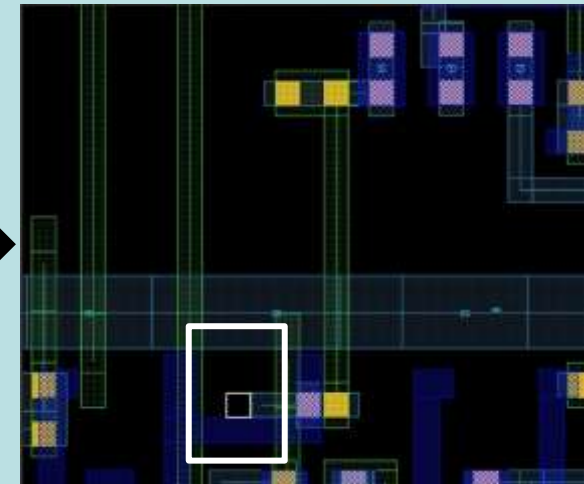
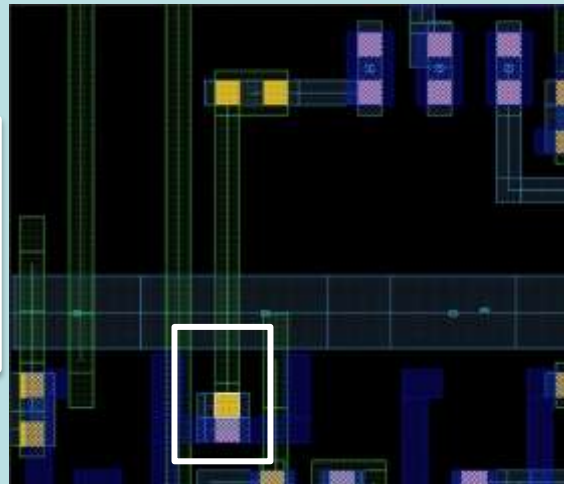
Automatic DRC Repair (ADR)

Automatically Find and Fix DRC Outliers

M6 Spacing Violation



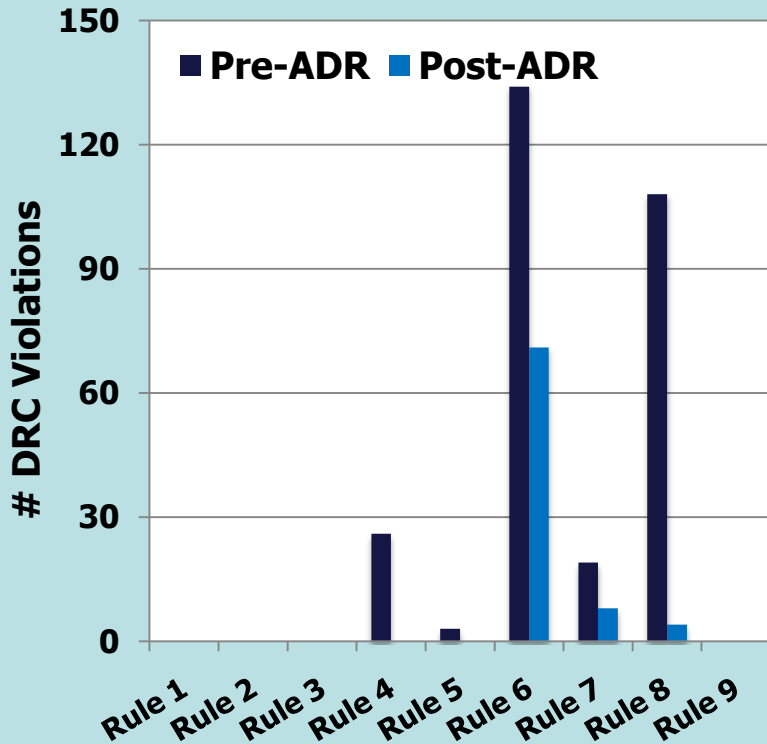
VIA2 Enclosure Violation



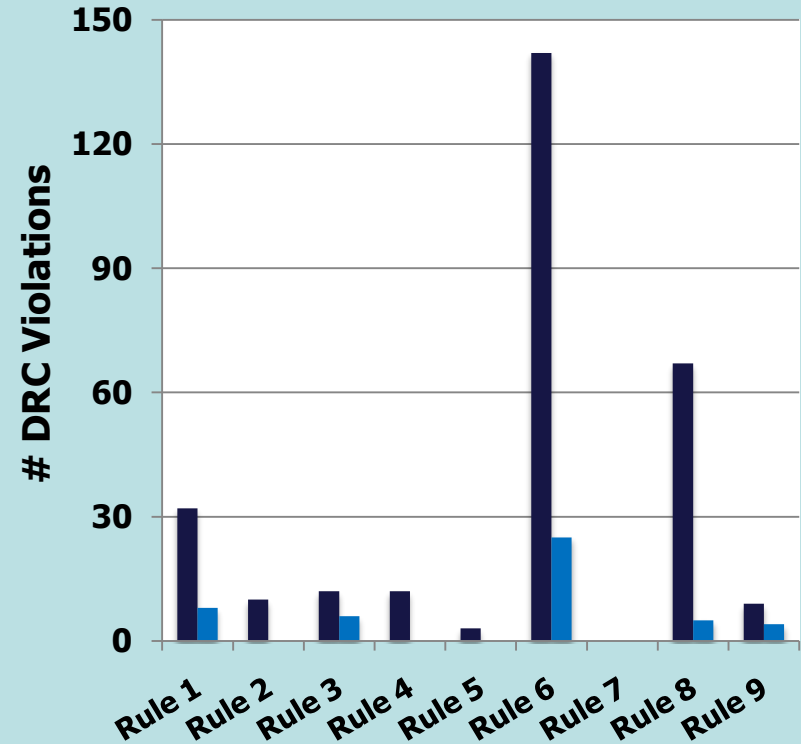
ADR Delivers Higher Productivity

Overall 80% Fix Rate

Block 1



Block 2



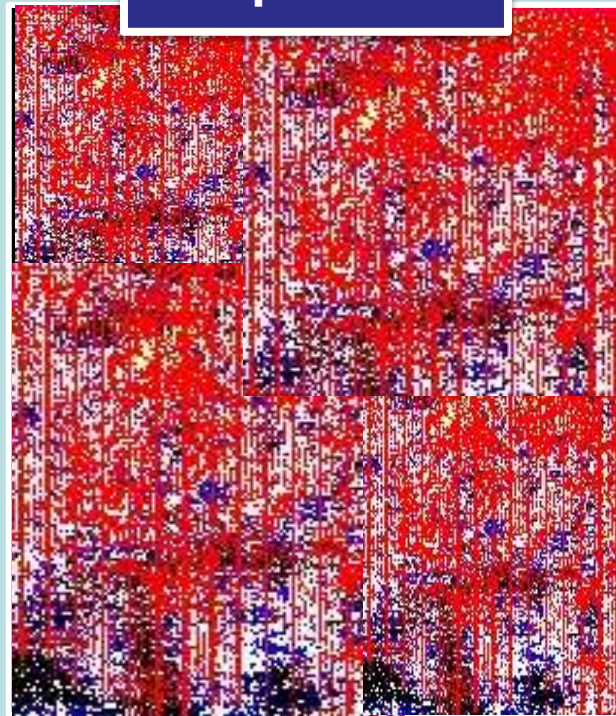
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Faster Full Chip Hierarchical Fill TAT

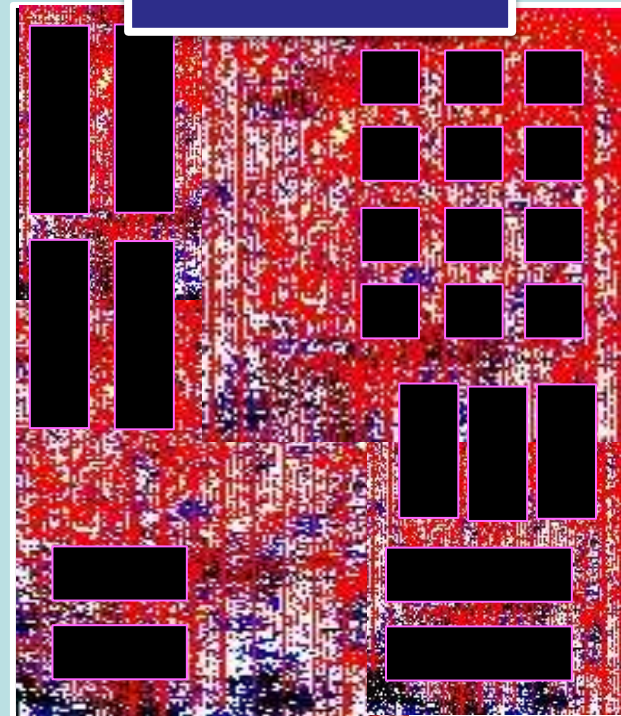
5x Faster Compared to Flat Fill

**Traditional Full
Chip Flat Fill**

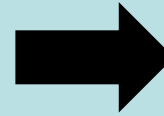


**12
Hours**

**IC Validator
Hierarchical Fill**



**2.5
Hours**



* Screenshots Only for Illustration Purposes

Summary: In-Design Physical Verification Deployment at Samsung

● Suggested Flow Enhancements

- More pre-route checks and API for user to define custom checks
- Enable automatic fixing for pre-route checks before place_opt
- Continue enhancing Automatic DRC Repair fix rates

● In-Design Physical Verification with IC Validator Delivering Automated and Predictable Design Closure

- Can save days with ADR for fixing DRC outliers
- Pre-routing verification eliminates late stage surprises
- Hierarchical, signoff metal fill
- Delivering block fill in minutes and 5x faster full chip fill