

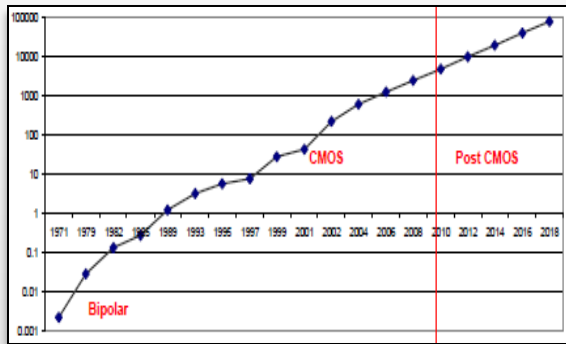
IC Compiler In-Design Technology

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Sr. Vice President and General Manager
Implementation Business Unit
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47th Design Automation Conference
14th June 2010

Emerging Design And Manufacturing Challenges

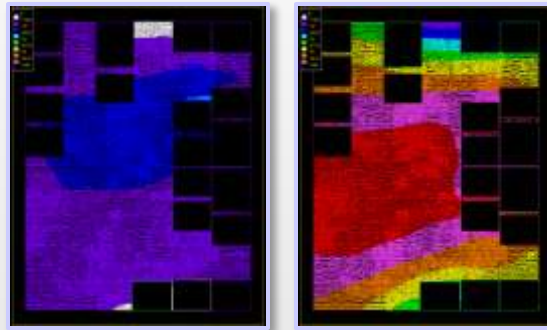
Growing Design Complexity



Long Live Moore's Law!
Source: Gartner 2009

2-3x every 2 years

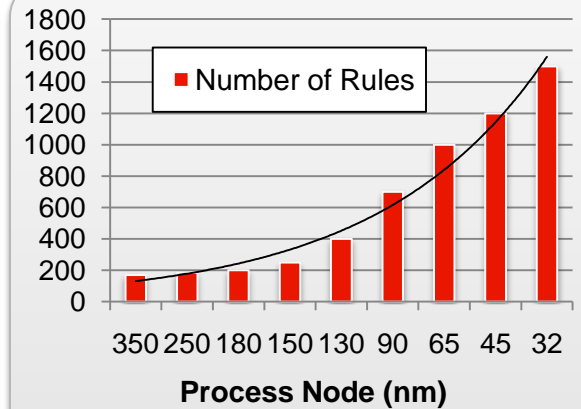
Harder Design Convergence



Voltage drop in 1st vs. nth mode

Complex multiple scenarios

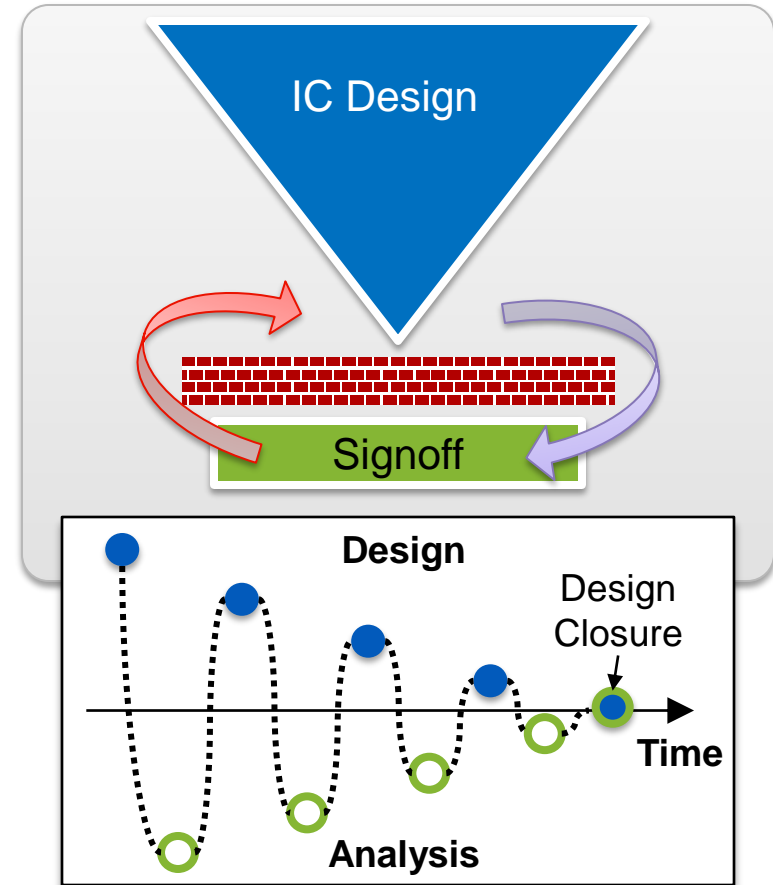
Rising Mfg. Compliance Needs



Difficult to write and maintain

Implement-Then-Verify Breaking Down

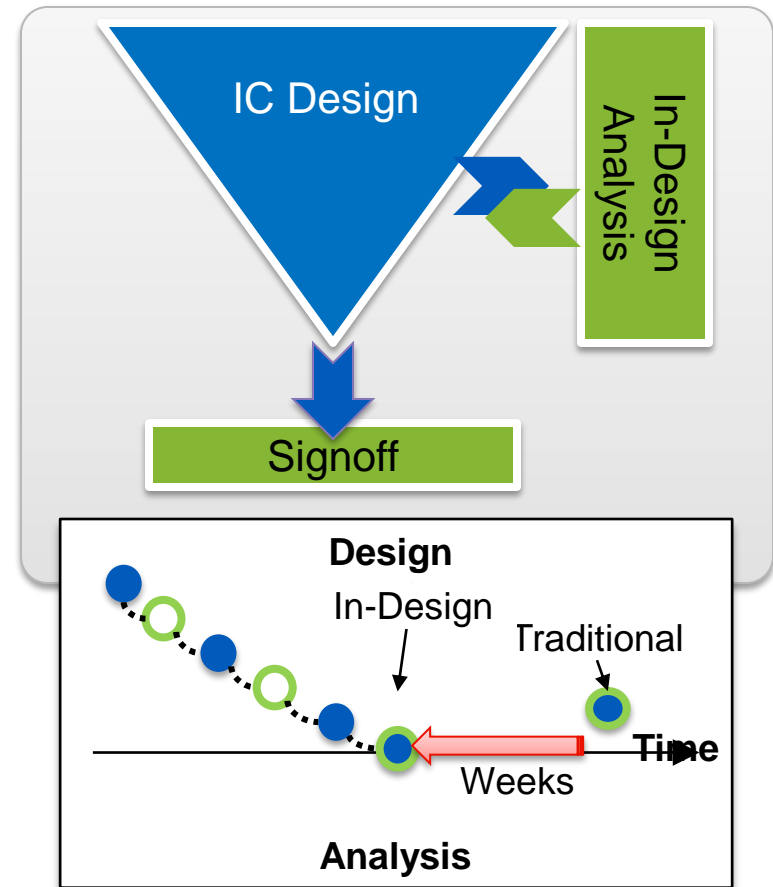
- Traditional approaches to design closure
 - Gated by analysis at signoff
 - Leads to unpredictable late-stage iterations
 - Delays tape-outs



Need To Integrate Signoff Analysis During Physical Design

In-Design Technology For Faster Design Closure

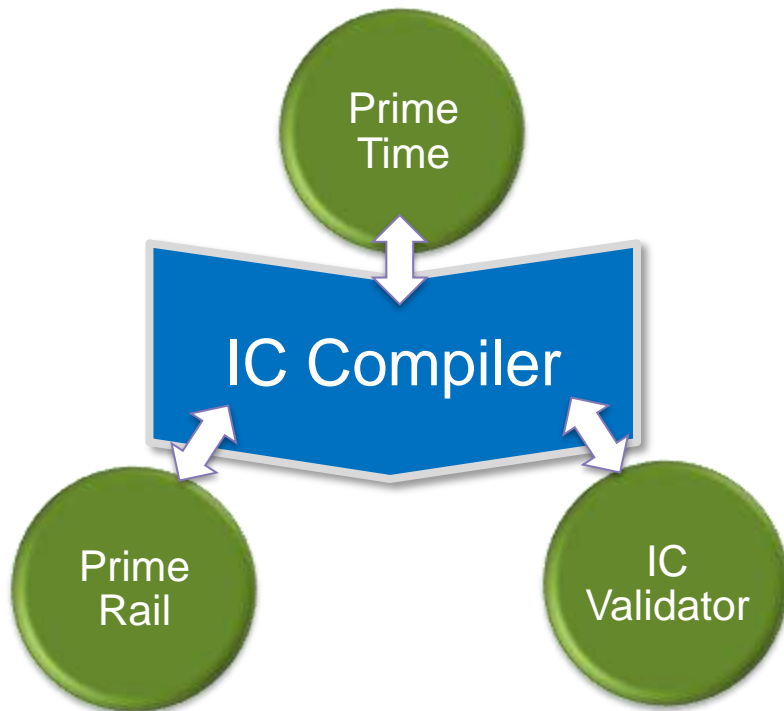
- Enables Early Fixes
- Eliminates Late-Stage Surprises
- Accelerates Overall Time-to-Tapeout



Avoid Costly Delays. Tape-out With Confidence.

IC Compiler In-Design Technology

Timing, P/G Analysis, Physical Verification



Best-In-Class
Place and Route

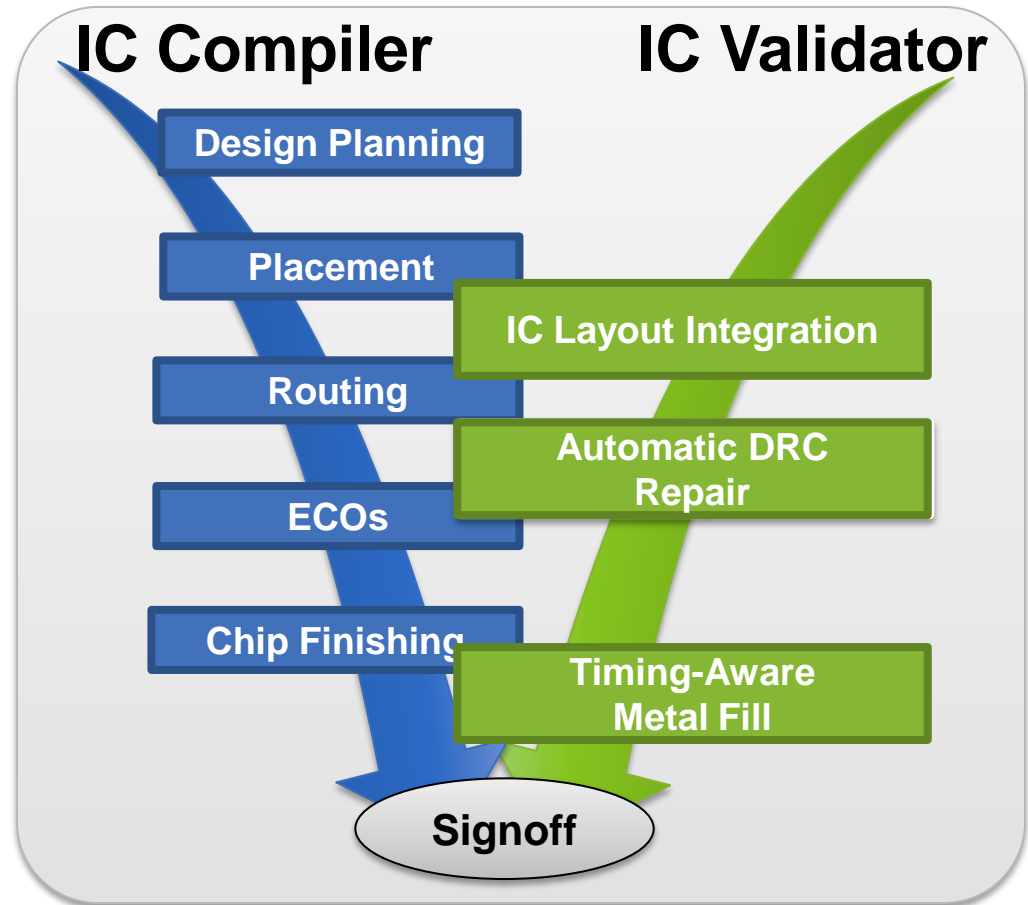
Signoff
Analysis Engines

Intelligent
Integration

A Shining Example Of In-Design

In-Design Physical Verification With IC Validator

- Enables Early Fixes
- Eliminates Late-Stage Surprises
- Accelerates Overall Time-to-Tapeout



A Theme You Will See Repeated Throughout This Luncheon